W-2W Current Steering DAC for Programming Phase Change Memory

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***Abstract* – This paper presents the design and experimental results of *W*-2*W* current mirror binary-weighted current steering Digital-to-Analog Converter (DAC) and its application for programming Phase Change Memory (PCM). This new approach significantly reduces the layout area of current-mode DACs by the virtue of its compact size. The proposed DAC can replace the write driver circuits in phase change memories. Both 6-bit and 12-bit DACs have been fabricated in 0.5 µm CMOS technology. The layout size of the 12-bit and the 6-bit DACs is 0.09 mm^2 and 0.04 mm^2 respectively. Experimental results are presented and the limitations are discussed.**

Keywords: binary-weighted, digital–to-analog converter (DAC), DNL, INL, mismatch, phase change memory, W-2W current mirror.

I. INTRODUCTION

Phase change memory (PCM) is considered to be a most suitable, unified solution for present day memory technologies. It exhibits superior performance when compared to Flash memory due to its scalability and fast read/write speeds [1]-[4]. PCM also provides a wide dynamic range of operation because of the potential for a large signal margin between the programmed (low resistance or SET) and erased (high resistance or RESET) states, providing the possibility of multi-level cell (MLC) operation [5]. Many approaches have been proposed to enhance the write performance and obtain a better distribution of resistance between SET and RESET states across the memory array for both single and multilevel cell operation [1]-[5]. This paper introduces the compact *W*-2*W* binary-weighted current steering Digital-to-Analog Converter (DAC) proposed to efficiently program the single and multi-level PCM cells.

II. W-2W CURRENT MIRROR

The *W*-2*W* current mirror is a novel and compact approach of implementing binary-weighted current steering DACs. It is utilized as the write driver circuit for programming phase change memory due to its compactness. Fig. 1 shows the implementation of a binary-weighted *W*-2*W* current mirror topology. It utilizes the fact that when two MOSFETs, with the same *W*/*L*, are connected in parallel, the result is an equivalent device of size 2*W*/*L,* while in series they are equivalent to a device of size *W*/2*L*. For the desired operation of the circuit the current flowing in M1 and M2 should be the same and equal to

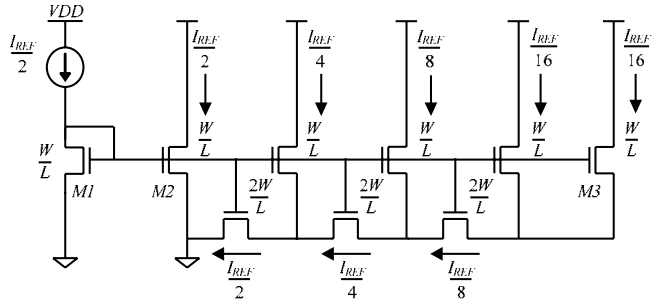


Figure 1. Binary-weighted current mirror, using *W*-2*W* topology [6].

the input current. The currents in the remaining devices should sum up to that input value or $I_{REF}/2$ in this case. The parallel and series combination of MOSFETs is further illustrated in Fig. 2. Thus looking at Fig. 1, simplifying the circuit from left to right, a string of MOSFETs can be combined into a single MOSFET with same size as M1 and M2 and having a drain current as $I_{REF}/2$ [6].

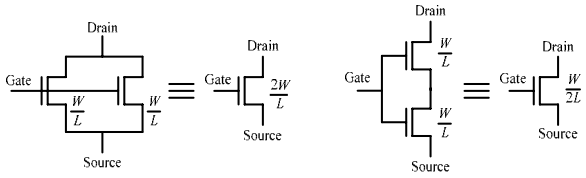


Figure 2. Parallel and Series MOSFETs [6].

The advantage of the *W*-2*W* topology over a traditional binary-weighted DAC circuit is the significant reduction in layout area for higher bit resolution because of the fewer number of devices employed. Assuming MOSFET only DAC, the area occupied by a device can be estimated as seen in (1), where η is the layout fill factor with $\eta < 1$

$$A_i = \frac{1}{\eta}\sum_i W_i L_i \tag{1}$$

Thus the ratio of conventional vs *W*-2*W*, N-bit binary weighted current steering DAC will be given by (2), where 2N/α account for switch size, where α is always > 1.

$$r = \frac{N\left(2^N - 1\right) + 2N/\alpha}{\left(3N - 1\right) + 2\left(N + 1\right)/\alpha} \tag{2}$$

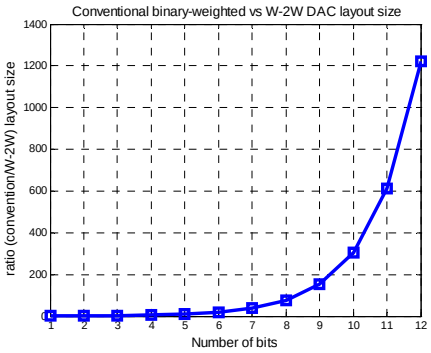


Figure 3. Plot showing the ratio (r) of the estimated layout areas for a conventional binary-weighted and the *W*-2*W* DAC vs the bit resolution.

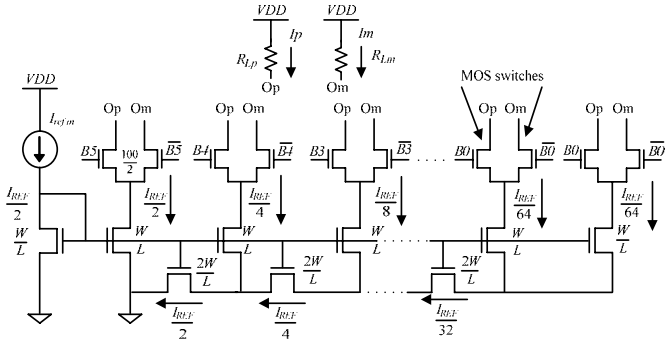
The unit size, *W*/*L*, device employed in the circuit helps in achieving a symmetrical layout which reduces the mismatch in the circuit due to process variations. It should be noted that in *W*-2*W* topology the MOSFETs operate with a continuous change from strong inversion region i.e. M1, M2, to the weak inversion region i.e. M3 [6].

III. THE CURRRENT STEERING DAC

From Fig. 1 it is seen that adding consecutive stages divides the reference current further by two, keeping the overall sum of currents equal to $I_{REF}/2$, that is, the same current that flows in M1 and M2. Both 6-bit and 12-bit binary-weighted current steering DACs are shown in Figs. 4 and 5. As seen in the figures, current is digitally steered to the output through the MOS switches. The first branch of the current mirror sinks $I_{REF}/2$, which is equivalent to the current DAC's MSB, while the last two branches sink $I_{REF}/2^N$.

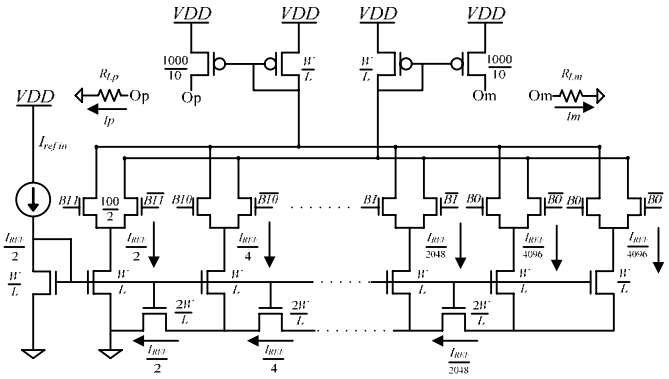
Instead of connecting the last two legs of the current mirror together and using a pair of switches, two pair of MOS switches can be used and connected to the same inputs $B0$ and $\overline{B0}$ in order to provide better matching between the current sources. An important thing to note here is that input reference current $I_{ref\ in}$ is equal to $I_{REF}/2$ as per the condition given in Sec. II, which is equal to MSB. The full scale or maximum output current (*Ip* or *Im*) is equal to (3) which is $2\times I_{ref\ in}$ (or $I_{REF}/2$), that is,

$$I_{FS(max)} = I_{REF} \tag{3}$$



NMOS W/L = 100/10

Figure 4. A 6-bit binary-weighted Current steering *W-2W DAC*.



NMOS & PMOS W/L = 100/10

Figure 5. A 12-bit *W-2W* DAC with amplifying PMOS current mirror.

A. The 6-bit DAC

Figure 4 shows the schematic of the 6-bit DAC. The digital inputs $B0-B5$, the reference current source $I_{ref\ in}$ and the differential output nodes O_p and O_m are all off chip. Inverted inputs $\overline{B0}-\overline{B5}$ are provided within the chip with the help of an inverter as seen in Fig. 6. Load resistance R_{Lp} and R_{Lm} are connected between O_p and O_m off chip pins and the power supply, *VDD*, respectively. The current I_p flows from zero, for all digital inputs at zeroes to full scale value $I_{FS\ (max)}$ for all inputs at ones and vice versa for I_m.

B. The 12-bit DAC

The 12-bit DAC employs PMOS current mirrors in addition to *W*-2*W* current mirrors, as seen in Fig. 5. This changes the current sunk by the NMOS devices into a current sink for the output of the DAC. It also isolates the drain of the digitally controlled switches from the load resulting in better matching by equalizing the NMOS's drain-source voltages used in the *W*-2*W* topology. The PMOS devices can further be used to distribute the current throughout the array by mirroring the current across the memory chip. In this case too, digital inputs $B0-B11$, the reference current source $I_{ref\ in}$ and the output nodes O_p and O_m are all off chip and inverted inputs $\overline{B0}-\overline{B11}$ are generated locally as discussed above. Load resistance R_{Lp} and R_{Lm} are connected to O_p and O_m, drain of amplifying PMOS(s). The amount of current I_p and I_m depends on the size selection of the amplifying PMOS; in this case it is ten times the width thus full scale current being $10I_{REF}$.

Since the load will be a phase change memory element with varying resistance and a DAC is being utilized for programming it to a SET or RESET state, we can control the programming current through the digital input code. In Figs. 4 and 5 the voltage drop across R_{Lp} and R_{Lm} (the PCM elements), when in SET or RESET state can not exceed above a certain value for a given set of programming currents. This is due to the reason that a large voltage drop across them will reduce the drain-source voltage across the MOSFETs which will affect the current mirror action in the circuit. In order to relax this constraint a pumped voltage V_{pmp} can be applied during system implementation as shown in Fig. 7. As seen in Fig. 8, the application of pumped voltage also overcomes the voltage drop due to parasitic bitline resistance in an array.

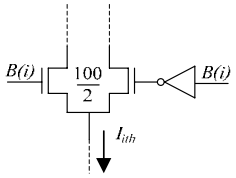


Figure 6. Inverter based scheme to provide differential input

C. Current source mismatch

The mismatch in current mirror will be due to threshold voltage mismatch between the devices and/or mismatch caused by β factor given in (4). The current flowing in the devices is approximated by square law equation (4) for long channel devices.

$$I_D = \frac{\beta}{2}\left(V_{GS}\text{-}V_{THN}\right)^2, \qquad \beta = \mu_n C'_{ox} \times \frac{W}{L} \tag{4}$$

The variance in the current due to mismatches can be derived as in (5) and stated in [8]

$$\frac{\sigma^2_{\Delta I_D}}{I_D{}^2} = \frac{\sigma^2_{\beta}}{\beta^2} + \frac{4\sigma^2_{V_{THN}}}{\left(V_{GS}\text{-}V_{THN}\right)^2} \tag{5}$$

thus from (5), the standard deviation for threshold voltage mismatch, σ_{VTHN} and β factor, σ_β is calculated as in (6), where $A_{V_{THN}}$ and A_β are process related constants [8].

$$\sigma_{V_{THN}} = \frac{A_{V_{THN}}}{\sqrt{W \times L}}, \qquad \sigma_\beta = \frac{A_\beta}{\sqrt{W \times L}} \tag{6}$$

Since the devices in the circuit are operating in both strong and weak inversion regions, it's important to mention that, the standard deviation parameters, equation (6) will hold in most cases [9], for weak inversion region also. From these equations it is clear that choosing large device will provide more accuracy, which will be important for linearity of the DAC. The unit element W/L chosen for DAC is 30 µm/3 µm.

D. INL and DNL

This section discusses the equations that govern the *W*-2*W* DAC's linearity. For a binary-weighted current steering DAC we assume that current source corresponding to the MSB, ($B_{N\text{-}1}$), has a maximum positive mismatch error and the remaining bits ($B0$ through $B_{N\text{-}2}$) have a maximum negative mismatch from ideal so that the errors sum to zero [7]. Thus the worst case INL for an N-bit DAC will be given by (7), where ΔI_K is the mismatch in current source and $|\Delta I_K|_{\max,\,INL}$ is the condition to keep the $INL < 0.5$ LSB.

$$\left|INL_{max}\right| = \frac{\Delta I_K}{2}, \qquad \left|\Delta I_K\right|_{max,INL} = \frac{I_{REF}}{2^N} \tag{7}$$

The DNL will be largest at midscale when the input transitions from 0111…11 to 1000...00. For the DNL to be < 0.5 LSB, the requirements for worst case current mismatch are more stringent than INL.

$$\left|DNL_{max}\right| = \Delta I_k\left(1\text{-}\frac{1}{2^N}\right), \qquad \left|\Delta I_K\right|_{max,DNL} = \frac{I_{REF}}{2^{N+1}\text{-}2} \tag{8}$$

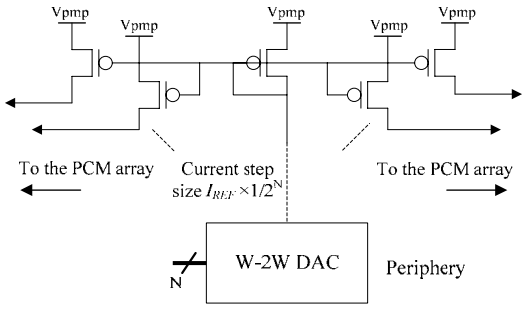


Figure 7. *W*-2*W* DAC implementation for programming a PCM array [1].

IV. PCM PROGRAMMING

Figure 7 shows a technique that can be employed to utilize the digitally controlled *W*-2*W* current steering as shown in [1] and discussed in Sec. IIIB. As stated in Sec. I, there are several algorithms [1]-[5] for RESET and SET operation of PCM elements in an array. In this section a simple scheme is proposed by utilizing the *W*-2*W* DAC as Write Driver (W/D) circuit to implement those algorithms.

A. SET Operation

A *long set sweep* current [1], SCD (stair case down) SET pulse programming [4], ASQ (arbitrary slow quench) [3] and/or MSPG (multiple step down pulse generation) [2] are different techniques for SET operation. These algorithms provide similar wave-shaping to SET current pulse and can be implemented through *W*-2*W* DAC. As mentioned in [5], tuning of *tail-end* of programming pulse for multilevel cell operation can also be achieved.

B. RESET Operation

For the RESET operation, the Cell Current Regulation (CCR) scheme [2] where RESET pulses of various amplitudes are required can be implemented with the help of *W*-2*W* DAC. It can also be used to generate the fast quench RESET current pulses.

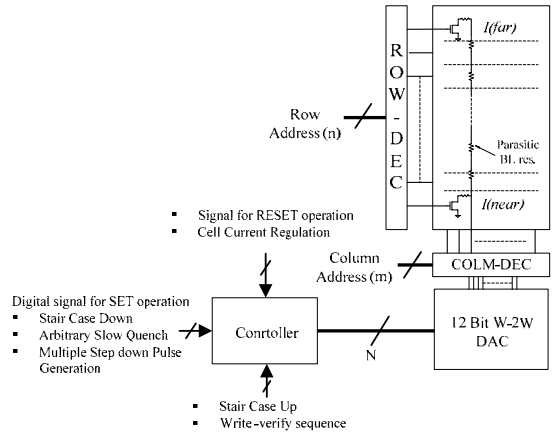


Figure 8. Block diagram of a possilbe PCM write operation [2].

The complete programming sequence, for example the SCU (stair case up) algorithm with preparatory sequence [1], or *write–verify* scheme mentioned in [3], can be easily generated

using the *W*-2*W* DAC. A simplified block diagram of PCM array programming, adapted from [2] is shown in Fig. 8 where 12-bit *W*-2*W* DAC is used for both SET and RESET operation.

Figure 9 shows the transient SPICE simulation of the signals generated for both SET and RESET operation, as mentioned in [1]-[5]. The duration of pulses for both SET and RESET current depends on the frequency of the digital input code. It can be observed from the simulation that DAC's output signal can be modulated to perform the *write-verify* as well as the *long set sweep* operation.

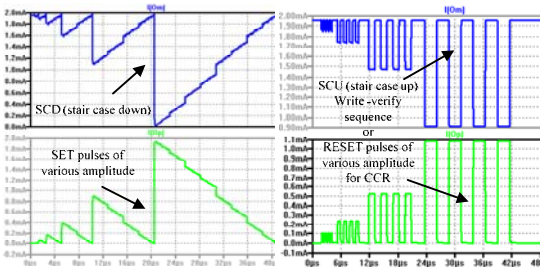


Figure 9. SET and RESET generation with controlled digital input

V. RESULTS

Figure 10 shows the test chip designed using ON Semiconductor's C5N (0.5 µm) process. The size of 12-bit DAC (a) is 0.0864 mm^2 and that of 6-bit (b) is 0.036 mm^2 roughly. The third part (c) is a test structure of *W*-2*W* current mirror as seen Fig. 1. Figure 11 shows the measured output of the 12-bit DAC obtained by cycling the DAC input using a 12-bit counter at 1 MHz, with $I_{ref\,in}$ 100 µA and load of 2.2 kΩ. Table 1 lists the DNL and INL data for test chip.

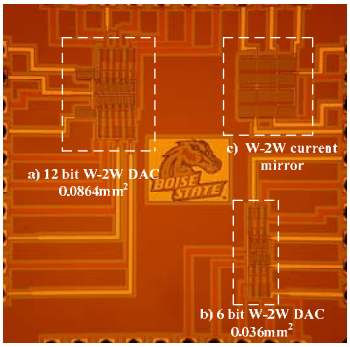


Figure 10. Microphotograph of test chip for *W*-2*W* DAC

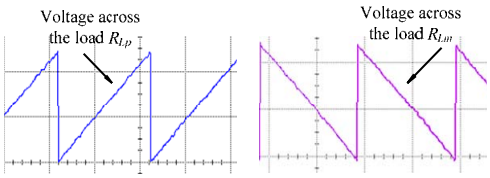


Figure 11. Scope capture of 12 bit *W*-2*W* DAC output obtained by cycling it through 12-bit binary counter at 1MHz.

TABLE I. CHIP TEST RESULTS

INL @1 MHz	DNL @1 MHz
Outp = ±0.95 LSB	Outp = 0.6 LSB
Outm = ±0.98 LSB	Outm= 0.87 LSB

VI. CONCLUSION

Both 12-bit and 6-bit *W*-2*W* DAC topologies were discussed and test results presented for the fabricated chip. In the case of a short channel process cascoded current source can be used to provide higher output resistance and hence a more idealistic current source. Using cascode structures will also reduce the parasitic capacitance's effects caused by varying output voltage. Based on the application of *W*-2*W* DAC as write driver circuit, its monotonicity will be more important then its large signal linearity (INL).

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REFERENCES

[1] Ferdinando Bedschi, et al., "A Multi-Level-Cell Bipolar- Selected Phas-Change Memory", International Solid-State Circuits Conference, pp. 428-42, 2008.

[2] Hyung-rok Oh, et al., "Enhanced Write Performance of a 64-Mb Phase – Change Random Aceess Memory", *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 122-126, January 2006.

[3] Kwang-Jin Lee, et al., "A 90nm 1.8V 512Mb Diode Switched PRAM with 266 MB/s Read Throughput", *IEEE Journal of Solid-State Circuits*, vol 43, pp. 150-162, January 2008.

[4] Ferdinando Bedschi, Chiara Boffino, Edoardo Bonizzoni, Claudio Resta, Guido Torelli, "Staricase-down SET programming apporach for phase-change memory" *Microelectronics Journal*, vol 38, pp. 1064-1069, 2007.

[5] T.Nirschl, et al., " Write Strategies for 2 and 4 –bit Multilevel Phase-Change Memory", *IEEE International Electron Devices Meeting*, pp. 461-464, December 2007.

[6] R. Jacob Baker, "CMOS Mixed-Signal Circuit Design," 1st ed.,*Wiley – IEEE*, 2002.

[7] R. Jacob Baker, CMOS Circuit Design , Layout and Simulation, 2nd ed., *Wiley- IEEE*, 2008.

[8] Marcel J. M. Pelgrom,C.J. Duinmaijer, Anton P.G. Welbers, " Matching Properties of MOS Transistors" , *IEEE Journal of Solid-State Circuits* , vol. 24, pp. 1433-1440,October 1989.

[9] Francesco Forti and Michael E. Wright, " Measurement of MOS Current Mismatch in the Weak Inversion Region" , *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 138-142, February 1994.